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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/923,225

08/06/2001

Stephen J. Plante

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09/13/2006

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EXAMINER

TORRES, JOSEPH D

ART UNIT

PAPER NUMBER

2133

DATE MAILED: 09/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Advisory Action
Before the Filing of an Appeal Brief**

Application No.

09/923,225

Applicant(s)

PLANTE ET AL.

Examiner

Joseph D. Torres

Art Unit

2133

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 28 August 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
(a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
(b) ☐ They raise the issue of new matter (see NOTE below);
(c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
The status of the claim(s) is (or will be) as follows:
Claim(s) allowed: _____.
Claim(s) objected to: _____.
Claim(s) rejected: 1-6, 18, 25 and 26.
Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:
See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____.
13. ☒ Other: See attached IDS filed 06/08/2006.

JOSEPH TORRES
PRIMARY EXAMINER

Joseph D. Torres, PhD
Primary Examiner
Art Unit: 2133

Continuation of 11. does NOT place the application in condition for allowance because: The Applicant contends, "Applicant submits that col. 1, lines 18-31 of Amon should be interpreted as describing operations that occur in three different single clock cycles, but those three single clock cycles are not consecutive clock cycles. As a result of this interpretation, Amon does not read on Applicant's claims. This interpretation is supported as follows".

The Examiner disagrees and asserts that the language in Amon should be interpreted exactly as Amon teaches. Amon explicitly uses first second and third clock cycles to describe the carrying out of functions. Col. 2, lines 46-52 in Amon explicitly teach a parallel data structure for the ACS butterfly operation allows the Viterbi decoding algorithm to be run faster and more efficiently on the data processing system by executing some of the instructions in parallel during the same clock cycle. The Examiner asserts that the process of adding a branch metric to the first path metric to obtain a first result and subtracting the branch metric from the second path metric to obtain a second result are combinational steps and neither adders nor subtractors are clocked device, that is; addition and subtraction are substantially instantaneous logic elements. It is clear from the context that Amon intends to include the addition and subtraction operations with the rest of the operations in the third clock cycle since they are required for the third clock cycle and since the adding and subtracting operations require the results of the second clock cycle.

The Applicant contends, "A loop execution time of 14 clock cycles is inconsistent with performing each of two instances of add, subtract and compare operations in a single clock cycle".

Col. 2, lines 30-38 in Amon teach that there are required processes for the ACS Butterfly operation subsequent to the third clock cycle.

The Applicant contends, "FIG. 5 illustrates a second embodiment of assembly code for implementing the ACS butterfly (col. 9, lines 37-49). Similarly to FIG. 4, add, subtract and compare instructions appear on second, third and fourth code lines, respectively of the main ACS loop. Amon states at col. 9, lines 45-46 that the assembly code of FIG. 5 permits one loop of the ACS butterfly to be performed in 10 clock cycles".

The Examiner asserts that the three clock cycles in col. 2, lines 20-30 in Amon correspond to Steps 101-105 in Figure 5. Only three of steps 101-105 (101, 102 and 105) require loading or reloading into memory. The rest of the operations in steps 101-105 are combinational logic operations, which occur substantially instantaneously in logic circuitry. Only the three memory operations in steps 101-105 require time. In steps 106-114, the seven (7) steps 106, 107, 108, 109, 111, 112 and 113 require storing, loading or reloading into memory all of which take time, i.e., at least one cycle..